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| 10/580,505 | 05/23/2006 | Jens Kristian Poulsen | 47161-00047USPX | 2345 |

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| EXAMINER | |
|---|---|
| ROBINSON, RYAN C | |
| **ART UNIT** | **PAPER NUMBER** |
| 4142 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/580,505 | POULSEN, JENS KRISTIAN | |
| | Examiner | Art Unit | |
| | RYAN C. ROBINSON | 4142 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/24/2006, 5/23/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-19 are pending in the current application.

2. The examiner acknowledges the preliminary amendments filed on 5/23/2006.

3. Claims 1-18 have been amended on 5/23/2006.

4. Claim 19 has been added on 5/23/2006.

### *Priority*

5. This application claims priority from PCT application number PCT/DK2004/000680, filed on 10/8/2004, which claims priority from provisional application number 60/525,039, filed on 11/24/2003.

### *Drawings*

6. The drawings filed on 5/23/06 are approved for examination purposes.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**8. Claims 1-4 and 6-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reesor, U.S. Publication No 2003/0235315, filed on 3/6/2003, (hereby Reesor), in view of Fujimori, U.S. Patent No 6,326,912, (hereby Fujimori), published on 12/25/2003.**

9. As to claim 1, Reesor discloses a "*digital microphone*" (Fig. 3) comprising: "*a microphone housing having a sound inlet*" (Fig. 2, element 3), and comprising: "*a transducer element*" (Fig. 3, element 2), "*comprising a displaceable diaphragm*" (Page 1, Para. 0004, line 10), "*and adapted to generate a transducer signal representative of sound received through the sound inlet*" (Page 2, Para. 0024, lines 1-3), "*an analog-to-digital converter*" (Fig 3, element 7), "*and an externally accessible terminal*" (Fig. 2, element 'DATA'), "*adapted to provide the unformatted single-bit output signal*" (Page 2, Para. 0022, lines 3-4).

It is noted, however, that Reesor does not specifically disclose that the analog-to-digital converter comprises "*a multi-level quantizer operatively coupled*" to the transducer element" *to convert the transducer signal into multi-bit samples*

*representative of the transducer signal, a digital signal converter adapted to convert the multi-bit samples into an unformatted single-bit output signal*", although Derunginsky does disclose that the analog-to-digital converter can comprise any suitable analog-to-digital converter (Page 3, Para. 0045).

On the other hand Fujimori discloses an analog to digital converter comprising "*a multi-level quantizer operatively coupled*" (Fig 1, element 16), "*to convert the transducer signal into multi-bit samples representative of the transducer signal*" (Col. 4, lines 1-2), the multi-bit digital signal corresponding to "*multi-bit samples*". There is "*a digital signal converter*" (Fig. 3, element 18) "*adapted to convert the multi-bit samples into an unformatted single-bit output signal*" (Col. 4, lines 5-7).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the analog-to-digital converter of Fujimori (Fujimori: Fig. 3, element 26), in the digital microphone of Reesor (Reesor: Fig. 3), because both Reesor and Fujimori are from the analog-to-digital conversion field. More specifically, Reesor is directed to a digital microphone with a built in analog-to-digital converter (Reesor: Abstract), while Fujimori is directed to an analog-to-digital converter having a multi-bit quantizer with a single-bit output (Fujimori: Abstract).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the analog-to-digital converter of Fujimori, in the digital microphone of Reesor, because that would have allowed users of Reesor's microphone to reduce noise (Fujimori: Col 4, lines 15-16), while still consuming minimal space (Fujimori: Col 4, lines 38-39).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the analog-to-digital converter of Fujimori, in the digital microphone of Reesor, because both Fujimori and Reesor teach methods of converting an analog signal to digital using delta-sigma modulation (Fujimori: Col. 1, lines 9-10; Reesor: Page 1, Para. 0007, lines 7-8), to achieve the predictable results of noise reduction and space efficiency.

10. As to claim 2, Reesor discloses a "*digital microphone*" (Fig. 3), "*wherein the analog-to-digital converter*" (Fig. 3, element 7), "*comprises an oversampled delta-sigma modulator*" (Page 1, Para. 0007, lines 7-8)

11. As to claim 3, Reesor discloses a "digital microphone" (Fig. 3), comprising an "*integral clock generator*" (Fig. 2, element "CLK") coupled to the "*analog-to-digital converter*" (Fig. 3, element 7).

It is noted, however, that Reesor does not disclose a "*digital signal converter*". On the other hand, Fujimori discloses a "*digital signal converter*" (Fig. 3, element 18).

12. As to claim 4, Reesor discloses "*a digital microphone*" (Fig. 3), "*wherein the microphone housing*" (Fig. 2, element 3), "*comprises a second externally accessible terminal for receipt of an external clock signal*" (Fig. 2, element 'CLK').

13. As to claim 6, Reesor discloses a "*digital microphone*" (Fig. 3), with an "*analog-to-digital converter*" (Fig. 3, element 7).

It is noted, however, that Reesor does not disclose that the analog-to-digital converter has "*a multi-level quantizer*", comprising "*between 3 and 64 discrete quantization levels*".

On the other hand, Fujimori discloses an analog-to-digital converter (Fig. 3, element 26), with "*a multi-level quantizer*", (Fig. 1, element 16), comprising "*between 3 and 64 discrete quantization levels*" (Col. 6, lines 25-27). Fujimori teaches that the multi-bit modulator can be implemented with numerous orders and stages, corresponding to "*between 3 and 64 discrete quantization levels*".

14. As to claim 7, Reesor discloses a "*digital microphone*" (Fig. 3), as well as an "*analog-to digital converter*" (Fig. 3, element 7).

It is noted, however, that Reesor does not disclose "*multi-bit samples*" provided by the analog-to-digital converter, "*represented in two's complement format.*"

On the other hand, Fujimori discloses that the "*multi-bit-samples*" (Col. 4, lines 1-2), are "*represented in two's complement format*" (Fig 9, element 80a). The input to the adder 80a, denoted by "M-BIT" is in "*two's complement format*".

15. As to claim 8, Reesor discloses a "*digital microphone*" (Fig. 3). It is noted, however, that Reesor does not disclose that the "*multi-bit samples generated by the multi-level quantizer are represented by a set of corresponding symbols, and wherein*

*each symbol comprises a number of one signs which is proportional with a magnitude of the corresponding multi-bit sample.*"

On the other hand, Fujimori discloses that the "*multi-bit samples generated by the multi-level quantizer*" (Col. 4, lines 1-2), "*are represented by a set of corresponding symbols, and wherein each symbol comprises a number of one signs which is proportional with a magnitude of the corresponding multi-bit sample*" (Col. 6, lines 3-5). Fujimori teaches that the stream of 1's and 0's is dependent on the magnitude of the analog signal, corresponding to "*a number of one signs which is proportional with a magnitude*".

16. As to claim 9, Reesor discloses a "*digital microphone*" (Fig. 3). It is noted however that Reesor does not disclose a "*multi-level quantizer*" comprising "*3 or 5 discrete quantization levels*".

On the other hand, Fujimori discloses *a multi-level quantizer*", (Fig. 1, element 16), comprising "*3 or 5 discrete quantization levels*" (Col. 6, lines 25-27). Fujimori teaches that the multi-bit modulator can be implemented with numerous orders and stages, corresponding to "*3 or 5 discrete quantization levels*".

17. As to claim 10, Reesor discloses "a digital microphone" (Fig. 3). It is noted, however, that Reesor does not disclose that the "*multi-level quantizer comprises N discrete quantization levels and each corresponding symbol comprises N-1 bits; N being an integer between 3 and 17*".

On the other hand, Fujimori discloses that the "*multi-level quantizer comprises N discrete quantization levels and each corresponding symbol comprises N-1 bits; N being an integer between 3 and 17*".

18. As to claim 11, Reesor discloses a "*digital microphone*" (Fig. 3). It is noted, however, that Reesor does not disclose that "*the digital signal converter comprises a delay circuit in cascade with an integer ratio upsampler.*"

On the other hand, Fujimori discloses a "*digital signal converter*" (Fig. 3, element 24), comprising a "*delay circuit*" (Col. 1, lines 49-51), FIR filter corresponding to a "*delay circuit*", in "*cascade with an integer ratio upsampler*" (Col. 1, lines 48-49). There is an interpolator (Fig. 3, element 24) which increases the sampling frequency, corresponding to "*upsampler*".

19. As to claim 12, Reesor discloses a "*digital microphone*" (Fig. 3), "*comprising a preamplifier interposed between the transducer element and the analog-to-digital converter*" (Fig. 3, element 5)

20. As to claim 13, Reesor discloses a "*digital microphone*" (Fig. 3), comprising an "*analog-to-digital converter*" (Fig. 3, element 7).

It is noted, however, that Reesor does not disclose "*an interpolator operatively coupled between the multi-bit samples provided*" by the analog-to-digital converter and "*the digital signal converter.*"

On the other hand Fujimori discloses "*an interpolator*" (Fig. 3, element 24) *operatively coupled between the multi-bit samples provided*" by the analog-to-digital converter (Fig. 3, element 16) and "*the digital signal converter*" (Fig. 3, element 18).

21. As to claim 14, Reesor discloses a "*portable communication device comprising a digitial microphone*" (Page, 2, Para. 27, lines 1-2), Reesor teaches that the digital microphone can be in a cellular phone, corresponding to a "*portable communication device*".

22. As to claim 15, Reesor discloses a "*monolithic integrated circuit for a miniature microphone*" (Page 1, Para. 0012, lines 3-5), the microphone is designed as a single integrated circuit, corresponding to a "*monolithic integrated circuit*". The circuit comprises "*a preamplifier adapted to provide an amplified transducer signal*" (Fig. 3, element 5) and "*an input section couplable to a miniature electret or condenser transducer element*" (Fig. 1, element 8), "*an analog-to-digital converter*" (Fig. 1, element 2), "*operatively coupled to the amplified transducer signal*" (Page 2, Para. 0024 lines 1-3). The preamplifier is disclosed as amplifying the transducer signal for the analog-to-digital converter, corresponding to "*operatively coupled*".

It is noted, however, that Reesor does not disclose that the microphone comprises "*a multilevel-quantizer*", and that the analog-to-digital converter is "*adapted to convert*" the amplified transducer signal into "*multi-bit samples representative of the amplified transducer signal, a digital signal converter adapted to convert the multi-bit*

*samples into an unformatted single-bit output signal, and an integrated circuit pad adapted to provide the single-bit output signal*".

On the other hand Fujimori discloses a "multilevel-quantizer" (Fig. 1, element 2), as well as an analog-to-digital converter "*adapted to convert*" the "*adapted to convert*" the amplified transducer signal into "*multi-bit samples representative of the amplified transducer signal*" (Col. 4, lines 1-2), the analog-to-digital converter first converts the analog signal to a multi-bit digital signal, corresponding to "*multi-bit samples*". There is a "*a digital signal converter*" (Fig. 3, element 18), "*adapted to convert the multi-bit samples into an unformatted single-bit output signal*" (Col. 6, lines 20-23). The incoming digital signal corresponds to "*the multi-bit samples*". There is "*an integrated circuit pad adapted to provide the single-bit output signal*" (Col. 3, lines 56-58). Fujimori discloses an output pin for a serial bit-stream, corresponding to a "*single-bit output signal*".

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the analog-to-digital converter of Fujimori (Fujimori: Fig. 3, element 26), in the digital microphone integrated circuit of Reesor (Reesor: Fig. 3), because both Reesor and Fujimori are from the analog-to-digital conversion field. More specifically, Reesor is directed to a digital microphone with a built in analog-to-digital converter (Reesor: Abstract), while Fujimori is directed to an analog-to-digital converter having a multi-bit quantizer with a single-bit output (Fujimori: Abstract).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the analog-to-digital converter of Fujimori, in the digital

microphone integrated circuit of Reesor, thereby reducing noise (Fujimori: Col 4, lines 15-16), while still consuming minimal space (Fujimori: Col 4, lines 38-39).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the analog-to-digital converter of Fujimori, in the digital microphone integrated circuit of Reesor, because both Fujimori and Reesor teach methods of converting an analog signal to digital using delta-sigma modulation (Fujimori: Col. 1, lines 9-10; Reesor: Page 1, Para. 0007, lines 7-8), to achieve the predictable results of noise reduction and space efficiency.

23. As to claim 16, Reesor discloses a "*monolithic integrated circuit*" (Page 1, Para. 0012, lines 3-5).

It is noted, however that Reesor does not disclose, that "*multi-bit samples generated by the multi-level quantizer are represented by a set of corresponding symbols, and wherein each symbol comprises a number of one signs which is proportional with a magnitude of the corresponding multi-bit sample*".

On the other hand, Fujimori discloses that the "*multi-bit samples generated by the multi-level quantizer*" (Col. 4, lines 1-2), "*are represented by a set of corresponding symbols, and wherein each symbol comprises a number of one signs which is proportional with a magnitude of the corresponding multi-bit sample*" (Col. 6, lines 3-5). Fujimori teaches that the stream of 1's and 0's is dependent on the magnitude of the analog signal, corresponding to "*a number of one signs which is proportional with a magnitude*".

24. As to claim 17, Reesor discloses a "*digital microphone*" (Fig. 3) "*wherein the analog-to-digital converter*" (Fig. 3, element 7), "*comprises an oversampled delta-sigma modulator*" (Page 1, Para. 0007, lines 7-8).

25. As to claim 18, Reesor discloses a "*monolithic integrated circuit*" (Page 1, Para. 0012, lines 3-5), with an "*analog-to-digital converter*" (Fig. 3, element 7).

It is noted, however that Reesor does not disclose "*the multi-level quantizer*" of the analog-to-digital converter "*comprises 3 or 5 discrete quantization levels*".

On the other hand, Fujimori discloses that "*the multi-level quantizer*" (Fig. 1, element 16) of the analog-to-digital converter "*comprises 3 or 5 discrete quantization levels*". (Col. 6, lines 25-27). Fujimori teaches that the multi-bit modulator can be implemented with numerous orders and stages, corresponding to "*3 or 5 discrete quantization levels*".

26. As to claim 19, Reesor discloses a "*digital microphone*" (Fig. 3). It is noted, however that Reesor does not disclose a "*digital signal converter*" that is a "*sigma delta signal converter*".

On the other hand, Fujimori discloses a "*digital signal converter*" (Fig. 3, element 18), that is a "*sigma-delta converter*" (Col. 4, lines 5-7).

**27. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reesor, U.S. Publication No 2003/0235315, filed on 3/6/2003, (hereby Reesor), U.S. Patent No 6,326,912, (hereby Fujimori), further in view of Tzartzanis et al. "Clock-Powered CMOS: A Hybrid Adiabatic Logic Style for Energy-Efficient Computing", published on 2/9/2000, (hereby Tzartzanis)**

28. As to claim 5, Reesor discloses a "*digital microphone*" (Fig. 3), and a "*microphone housing*" (Fig. 2, element 3), and an "*analog-to-digital converter*" (Fig. 3, element 7).

It is noted, however, that both Reesor, Fujimori do not disclose a "*DC voltage generating means disposed within*" the microphone housing, "*and operatively coupled to the external clock signal so as to derive a DC voltage supply for operating at least the* analog-to-digital converter, although Reesor suggests a DC voltage supply to the digital microphone device as detailed in (Fig. 2, element 'VDD'), VDD corresponding to DC voltage.

On the other hand, Tzartzanis discloses a "*DC voltage generating means disposed within*", (Page 2, Section 2, lines 6-7). Tzartzanis discloses a means of powering logic circuits by means of storing power from the clock signal in E-R latches. The E-R latches correspond to "*DC voltage generating means*". The voltage generating means is "*operatively coupled to the external clock signal so as to derive a DC voltage supply*" (Page 2, Section 2, lines 4-7). Tzartzanis teaches that the clock driver does not

necessarily have to be on the same chip as the clock-powered logic, corresponding to an "*external clock signal*".

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use Tzartzani's technique of powering the device by the clock signal (Tzartzani: Page 2, Section 2, lines 4-7), in the digital microphone of Reesor (Reesor: Fig. 3), thereby reducing circuitry overhead (Tzartzani: Page 2, Section 1, line 9), and offering high energy efficiency (Tzartzani: Page 1, Section 1, lines 15-16).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use Tzartzani's technique of powering the device by the clock signal, in the digital microphone of Reesor, to achieve the predictable results of reducing circuitry overhead, thereby saving space, and energy efficiency.

## *Conclusion*

The prior art made of record

| | | |
|---|---|---|
| a. | U.S. Publication Number | 2003/0235315 (Digital Microphone) |
| b. | U.S. Patent Number | 6326912 (A/D conversion) |
| c. | Publication | Tzartzanis et. al, *"Clock Powered CMOS"* (Logic devices powered from clock signal) |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan C. Robinson whose telephone number is (571) 270-3956. The examiner can normally be reached on Monday through Friday from 9 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Srirama Channavajjala, can be reached on (571) 272-4108. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Robinson

***/Srirama Channavajjala/***

***Supervisory Patent Examiner, Art Unit 4142***